**Experiment 2: CMOS Transistor Level**

**Current Source**



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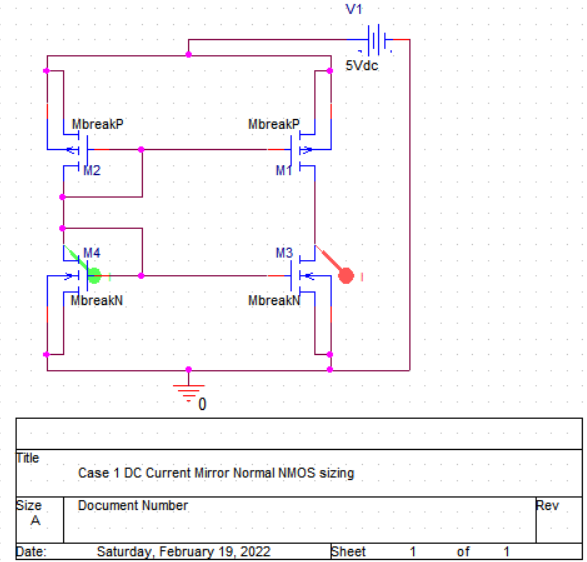
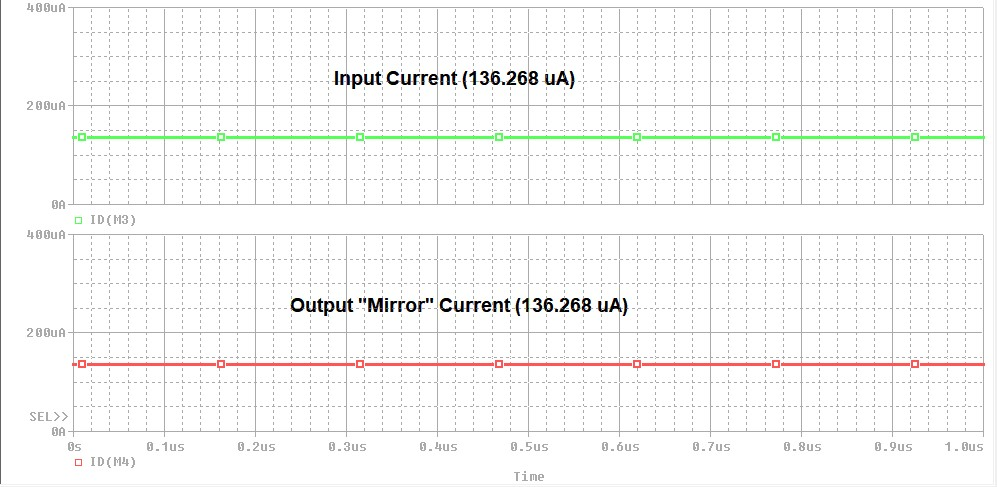
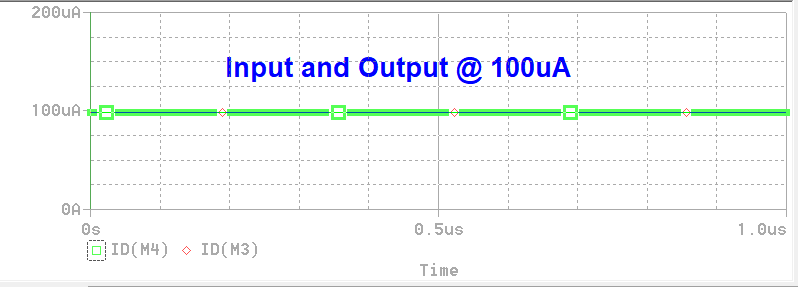


Figure 2.1: Case 1 CMOS Mirror Normal Sizing



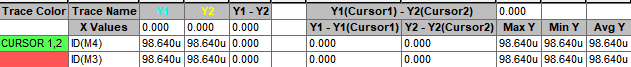




Figure 2.2: Graphical representation of CMOS Mirror with Normal Sizing

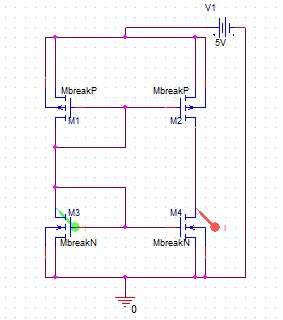
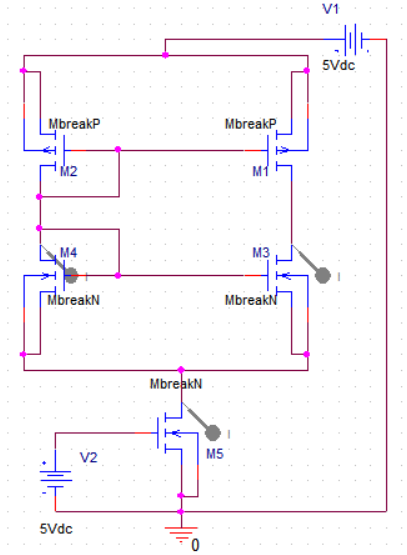


Figure 2.3: **Case 2** DC Current Mirror with Double NMOS sizing schematic

Figure 2.4: DC Current Mirror with Double NMOS sizing waveform and cursor, I/O current @ 136.268 uA



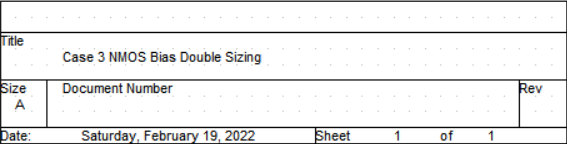
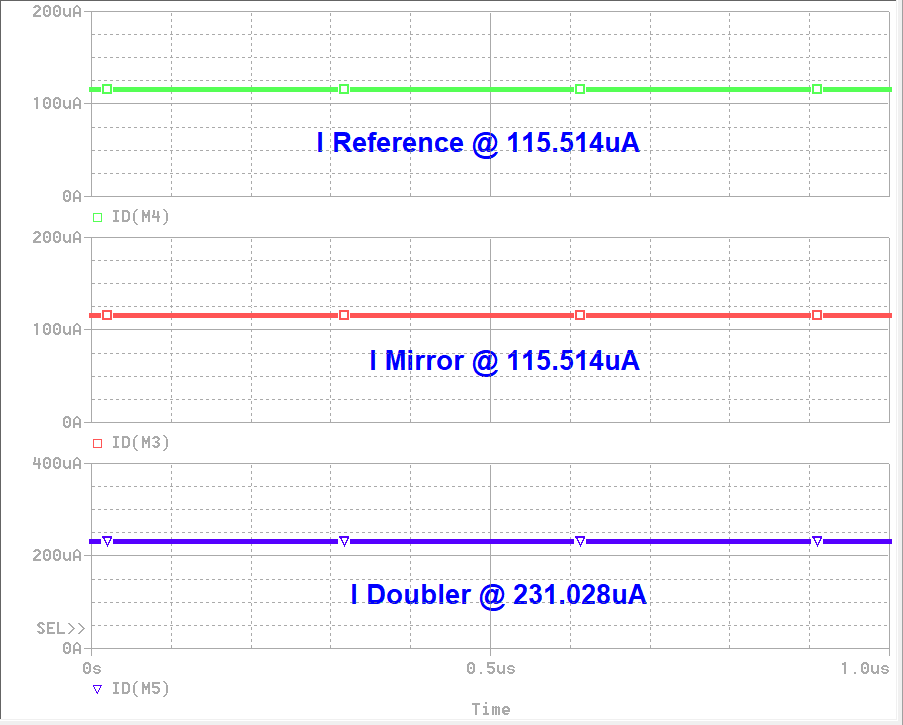


Figure 2.5: Case 3 NMOS Bias Double Sizing

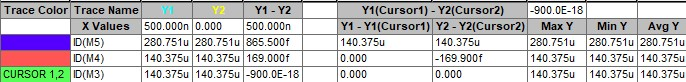
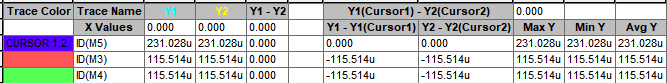


Figure 2.6: Waveform of NMOS Bias Double Sizing

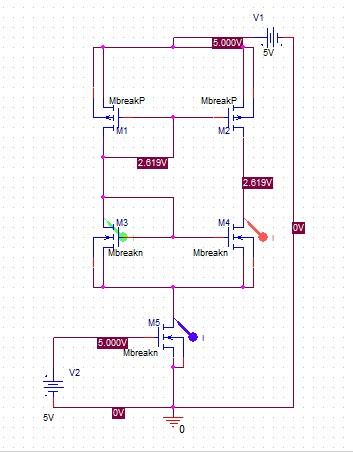


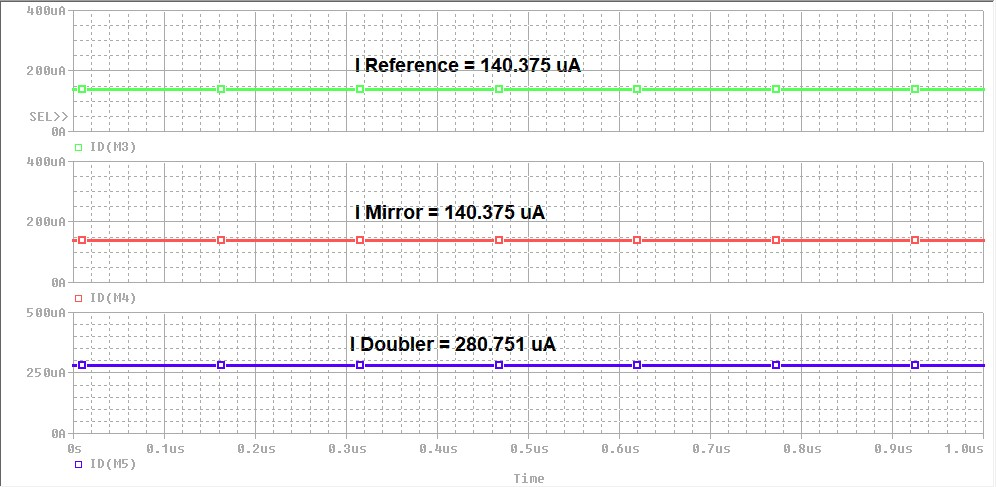
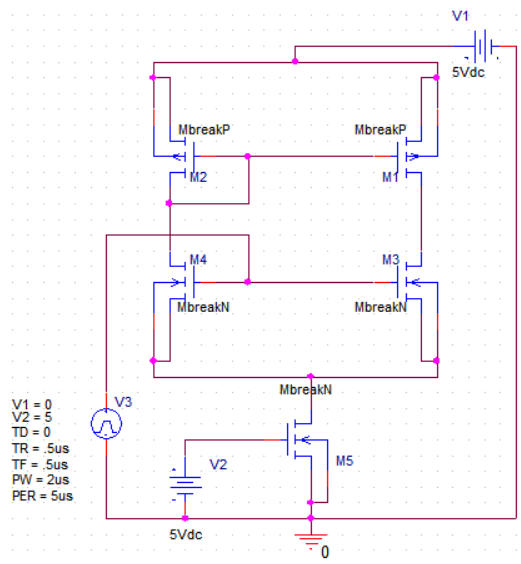
Figure 2.7: **Case 4** DC Current Mirror with Bias NMOS and 3 \* (W/L) for NMOS sizing schematic

Figure 2.8: DC Current Mirror with Bias NMOS and 3 \* (W/L) for NMOS sizing waveform and cursor. Reference and Mirror currents @ 140.375 uA and Doubler current @ 280.751 uA



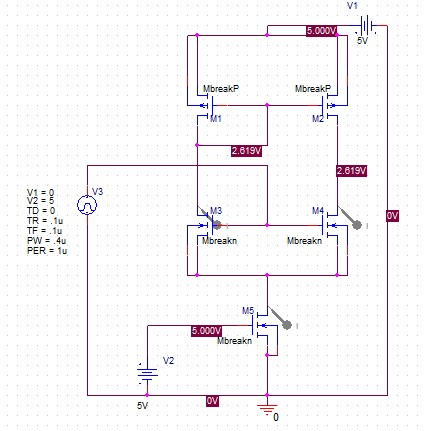


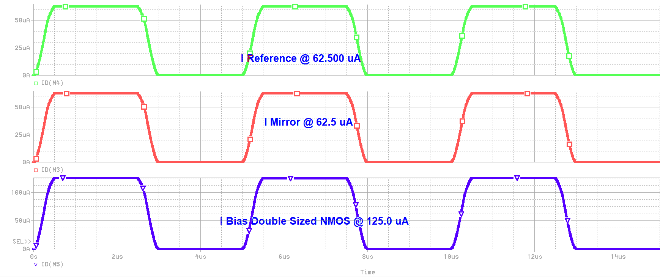
Figure 2.9: Case 5 AC Current Mirror with Bias NMOS @ 2(W/L) @ 200kHz

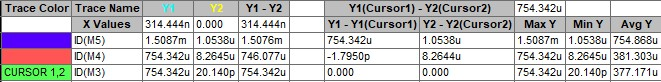
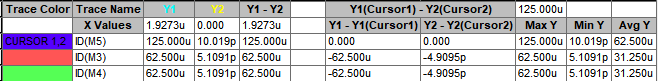
Figure 2.10: Graphical representation of AC current Applied to Double Sized Biased NMOS Circuit

Figure 2.11: **Case 6** AC Current Mirror with Bias NMOS and 2 \* (W/L) for NMOS sizing schematic, v\_in(t) = 5V square wave with f = 1 MHz

Figure 2.12: AC Current Mirror with Bias NMOS and 2 \* (W/L) for NMOS sizing waveform, v\_in(t) = 5V square wave with f = 1 MHz.Reference and Mirror currents @ 754.342 uA and Doubler current @ 1.5087 mA